

Amendments to the Claims

This listing of claims will replace all prior listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A manufacturing method of a semiconductor wafer, wherein an epitaxial layer is grown in a trench of a semiconductor wafer having a trench structure by gradually reducing a temperature in a temperature range of 400 to 1150°C ~~or by gradually reducing a temperature~~ and then lowering the temperature at a ~~predetermined speed rate of 1 to 100°C/min~~ based on a vapor growth method while supplying a silane gas as a raw material gas, thereby filling the epitaxial layer in the trench.

2., 3. (Cancelled)

4. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 1, comprising:

a step of forming a first layer on an inner surface of the trench of the semiconductor wafer at a first temperature in the range of 900 to 1150°C by the vapor growth method;

a step of forming a second layer on a surface of the first layer in the trench at a second temperature in the range of 850 to 1100°C lower than the first temperature by the vapor growth method; and

a step for forming a third layer on a surface of the second layer in the trench by the vapor growth method while reducing a temperature from the second temperature at a ~~speed rate of 1 to 100°C/min~~ so that the epitaxial layer consisting of the first layer, the second layer and the third layer is filled in the trench.

5. (Previously Presented) The manufacturing method of a semiconductor wafer according to claim 1, comprising:

a step of forming a first layer on an inner surface of the trench of the semiconductor wafer at a first temperature in the range of 900 to 1150°C by the vapor growth method;

a step of forming a second layer on a surface of the first layer in the trench at a second temperature in the range of 850 to 1100°C lower than the first temperature by the vapor growth method;

a step of forming a third layer on a surface of the second layer in the trench at a third temperature in the range of 800 to 1050°C by the vapor growth method; and

a step of forming a fourth layer on a surface of the third layer in the trench by the vapor growth method while reducing a temperature from the third temperature at a speed rate of 1 to 100°C/min so that the epitaxial layer consisting of the first layer, the second layer, the third layer and the fourth layer is filled in the trench.

6., 7. (Canceled)

8. (Currently Amended) The manufacturing method of a semiconductor wafer according to claim 2 4, wherein, when the semiconductor wafer is left in the air for eight hours or more in a state where the trench has been formed in the semiconductor wafer or in a state where the first layer, the second layer or the third layer has been formed on the inner surface of the trench, the semiconductor wafer is dipped in a mixture of an alkaline water solution and hydrogen peroxide solution having an etching rate of 0.1 to 1 nm/min for 1 to 10 minutes and cleansed, and then the semiconductor wafer is dipped in fluorinated acid for 0.1 to 60 minutes and cleansed.

9. (Previously Presented) The manufacturing method of a semiconductor wafer according to claim 8, wherein the semiconductor wafer is dipped in an acidic or alkaline etchant having an etching rate of 0.1 to 1 $\mu\text{m}/\text{min}$ for 0.1 to 10 minutes to increase a width of the trench before forming the third layer or the fourth layer required to completely fill the inside of the trench of the semiconductor wafer.

10. (Original) The manufacturing method of a semiconductor wafer according to claim 1, wherein a temperature at which the epitaxial layer is grown by the vapor growth method falls within a range of 650 to 950°C.

11. (Original) The manufacturing method of a semiconductor wafer according to claim 1, wherein a temperature at which the epitaxial layer is grown by the vapor growth method falls within a range of 400°C to 650°C.

12. (Canceled)

13. (Previously Presented) The manufacturing method of a semiconductor wafer according to claim 4, wherein a thickness w_1 of the first layer is $(W/20) \leq w_1 \leq (W/10)$, a thickness w_2 of the second layer is $(W/10) \leq w_2 \leq (W/5)$, and the remainder is the third layer, where W is a width of the trench.

14. (Previously Presented) The manufacturing method of a semiconductor wafer according to claim 5, wherein a thickness w_1 of the first layer is $(W/20) \leq w_1 \leq (W/10)$, a thickness w_2 of the second layer is $(W/10) \leq w_2 \leq (W/5)$, a thickness w_3 of the third layer is $(W/10) \leq w_3 < (W/5)$, and the remainder is the fourth layer, where W is a width of the trench.

15.-24. (Canceled)